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ATX:230mm*185mm

Intel -CoffeeLake-S plamform

CPU:
LGA1151
*CPU POWER PAK *4Phase*
*GT POWER PAK *2 Phase*

System Chipset:
H310C

Onboard Chip:
SIO: NUVOTON 5567
HD Audio Codec: ALC887
LAN: INTEL I219V
Flash ROM: SPI 64 MB

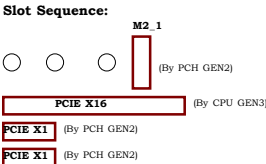
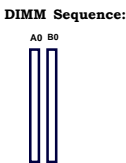
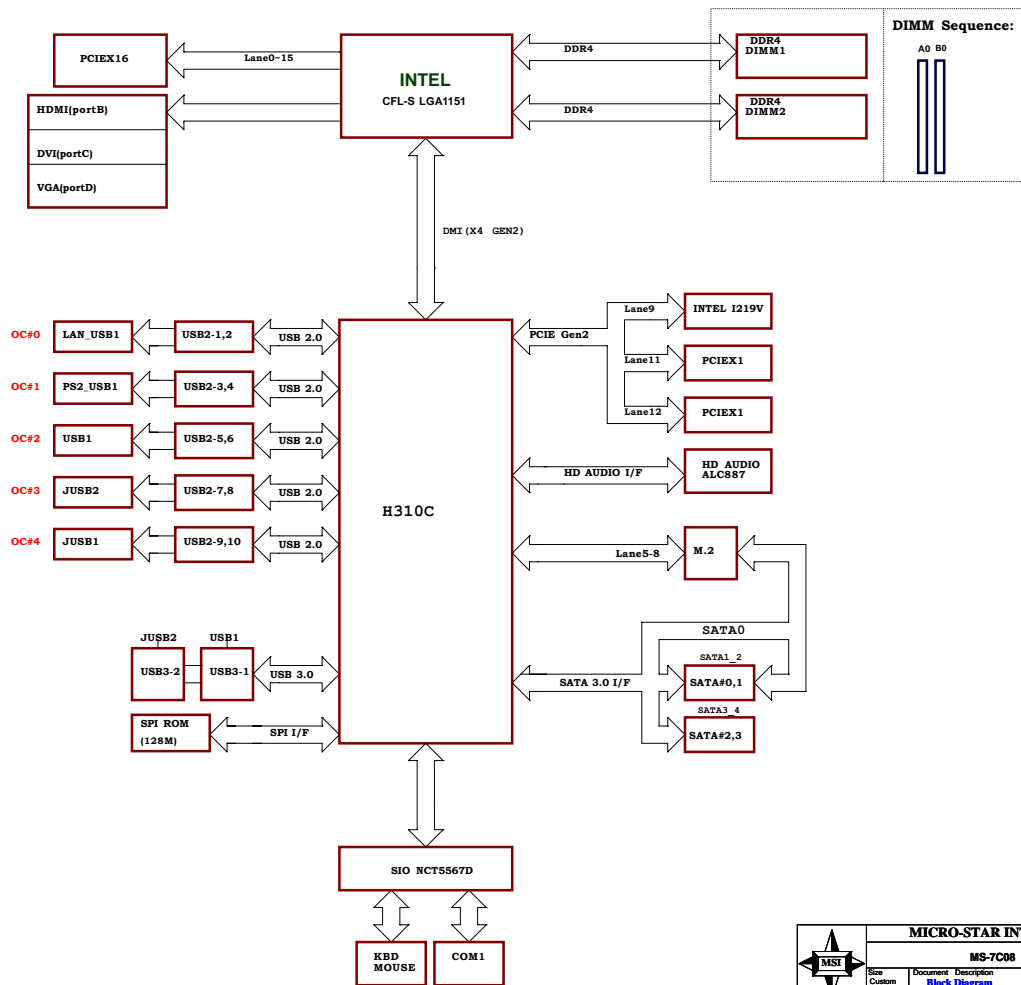
PWM:
VCORE - RT3607 138A
VGT- RT3607 45A
DDR - RT8231 11.525A
DDR VPP25- MP2143 1.12A
PCH(1.0V) - RT8125E 10.743A
VCCSA - RT8125E 11.1A
VCCIO - SY8288 6.4A

Main Memory:
*DDR4 * 2 (Dual Channel)*

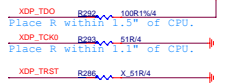
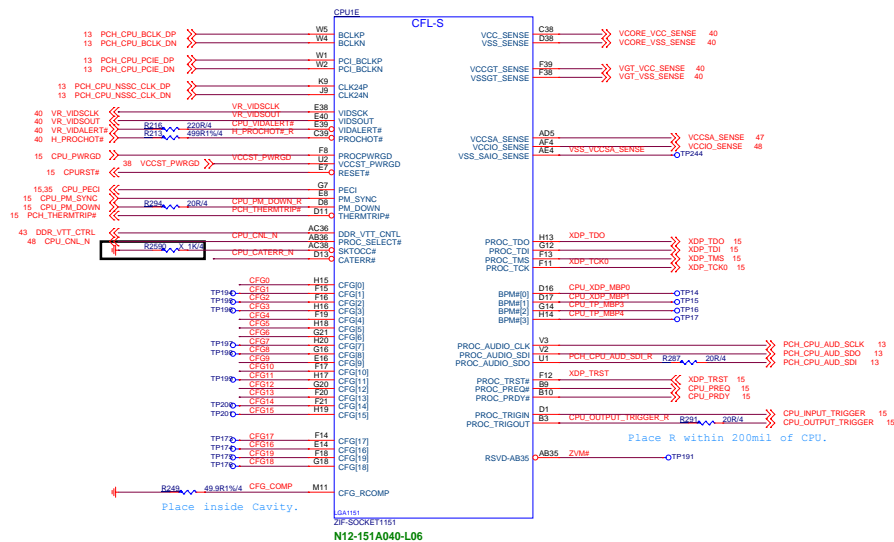
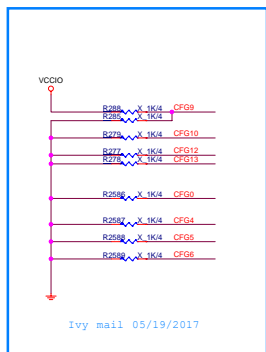
ACPI:
5VDAUL:uP7501
5VDIMM:uP7501
3VSB:MP2147
3VDSW:GS7133
VCCSTPLL:GS7133

Expansion Slots:
*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 2*

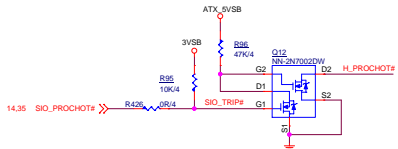
Block Diagram







CFG Table			
	HIGH	LOW	DESCRIPTION
0	NO LOCK	LOCK	PCU PLL LOCK
1			SEVD
2	NOHW	REVERSE	FEL LANE REVERSAL
3			SEVD
4	DISABLE	ENABLE	eCP
5	DISABLE	ENABLE	FEUDCFGSEL[0]
6	DISABLE	ENABLE	FEUDCFGSEL[1]
7	RESET#	SDIO REQ	FEU CEFER TRAINING
8			SEVD
9			SEVD
10			SEVD
11			SEVD
12			SEVD
13			SEVD
14	SEVD		
15	SEVD		



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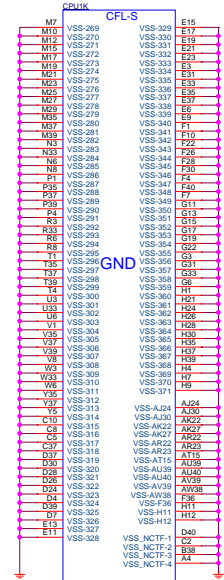
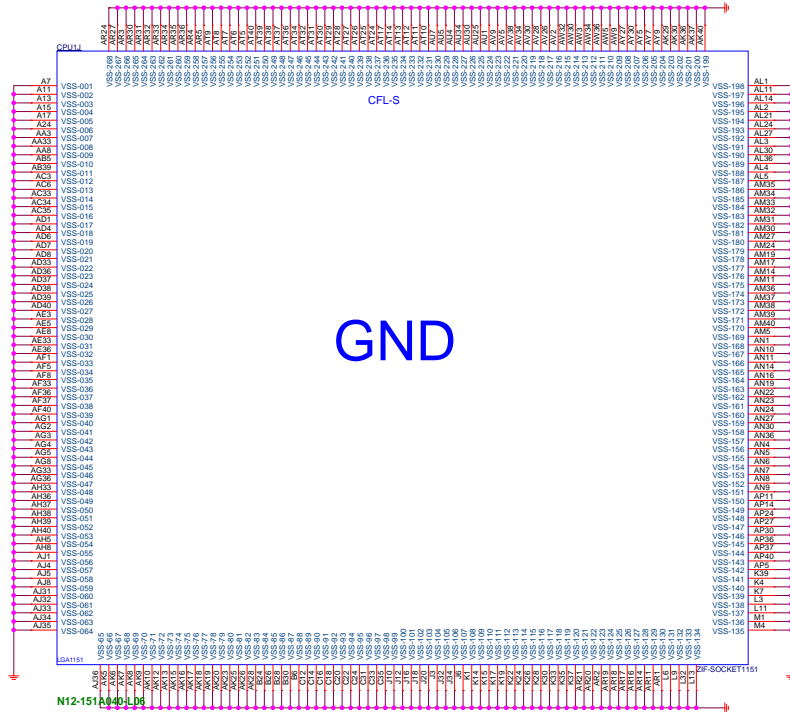
Size Custom	Document Description CPU-Control/MISC/CFG/Audio	Rev 1.0
Date: Wednesday, May 23, 2018		Sheet 5 of 60

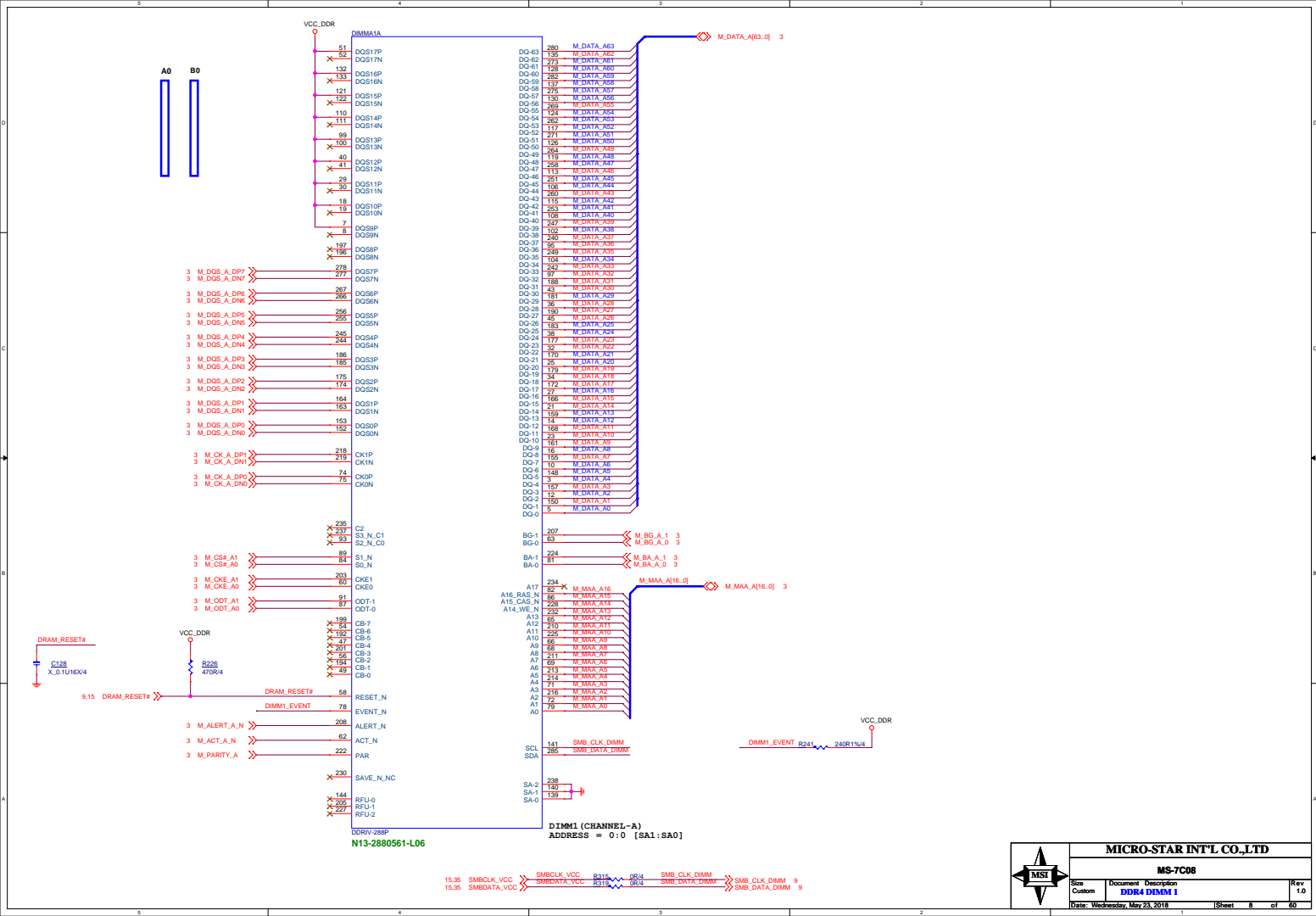


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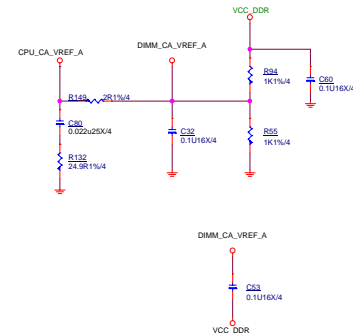
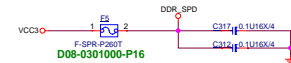
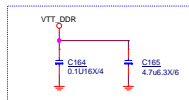
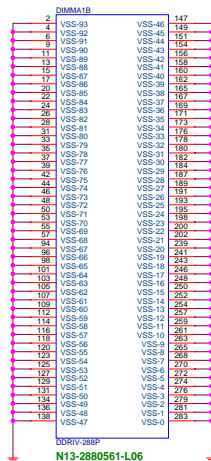
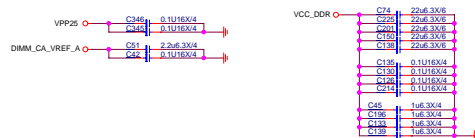
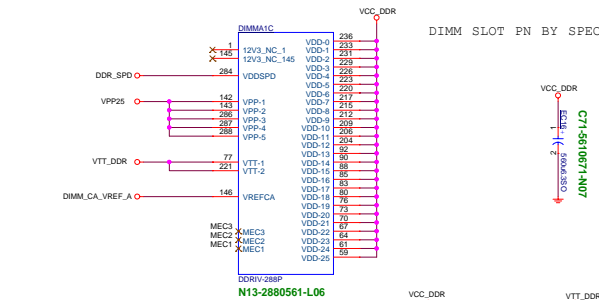
Size Custom	Document Description CPU-Power
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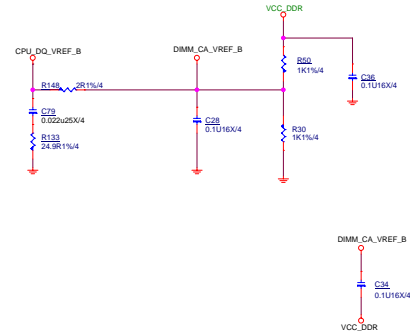
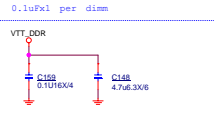
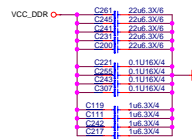
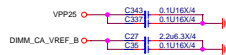
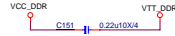
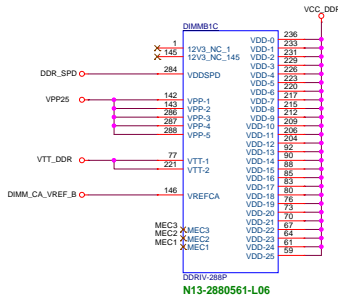
Date: Wednesday, May 23, 2018 Sheet 6 of 60

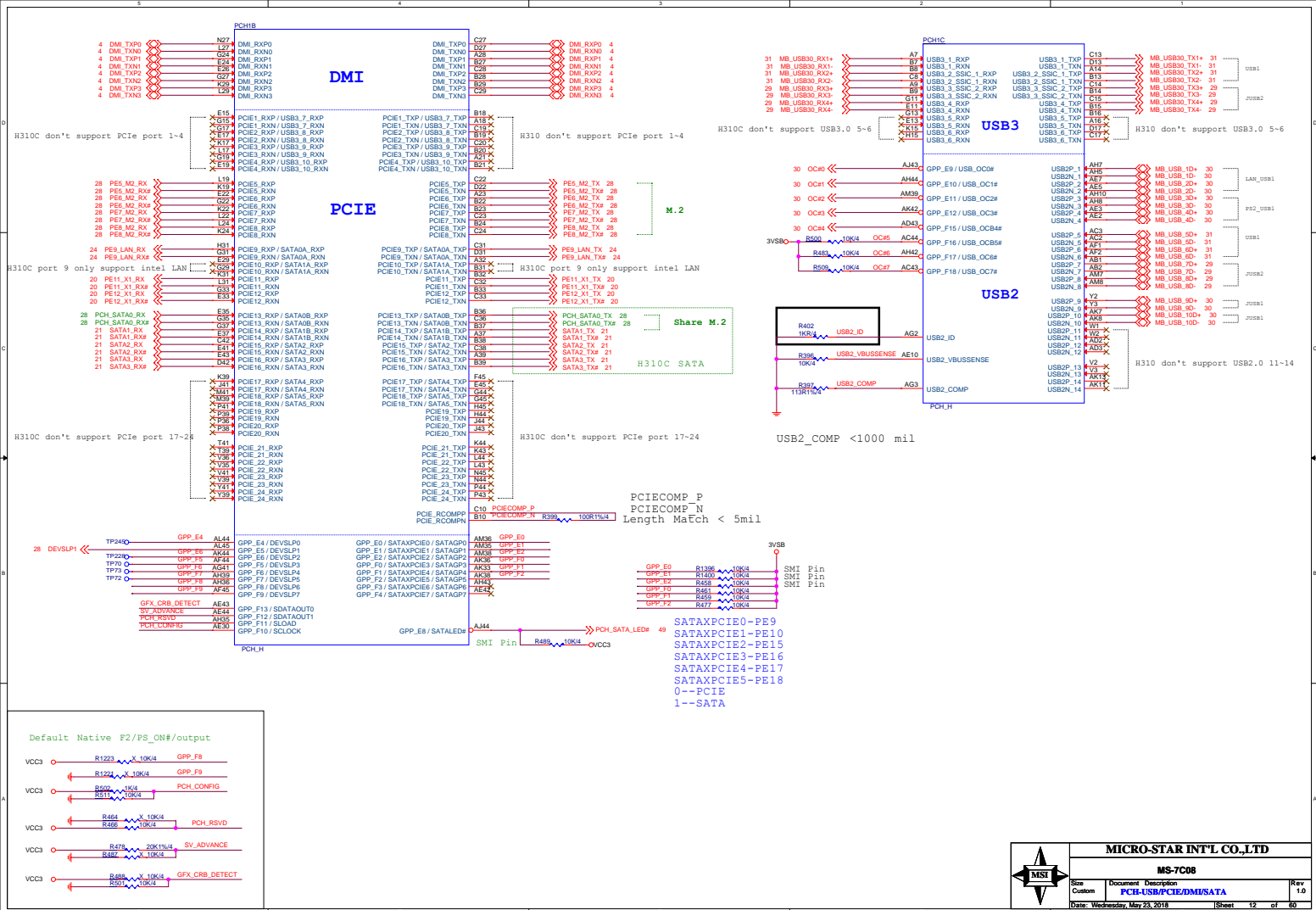




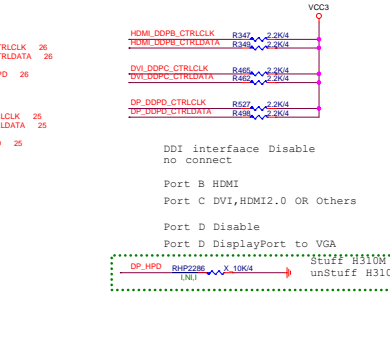
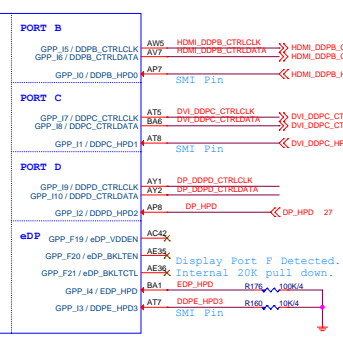
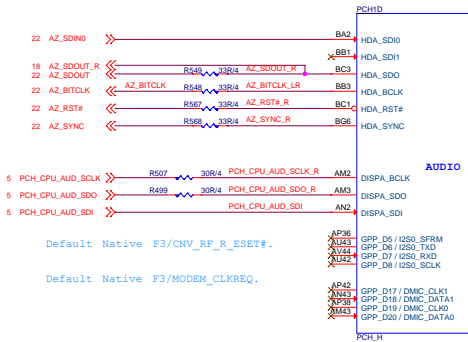
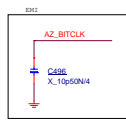
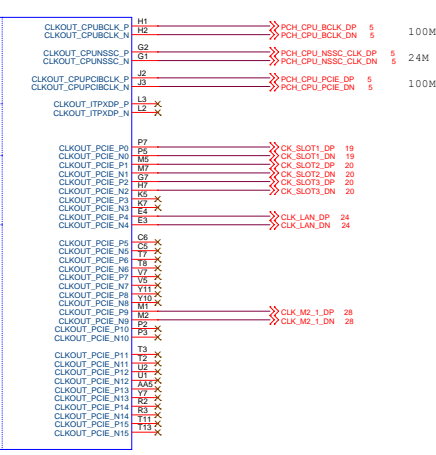
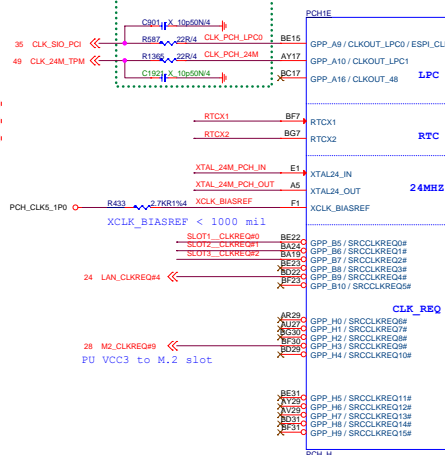
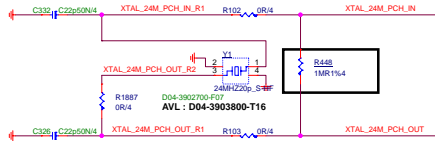
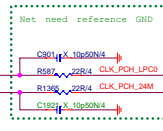
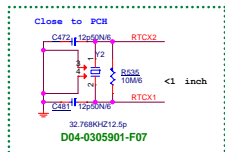




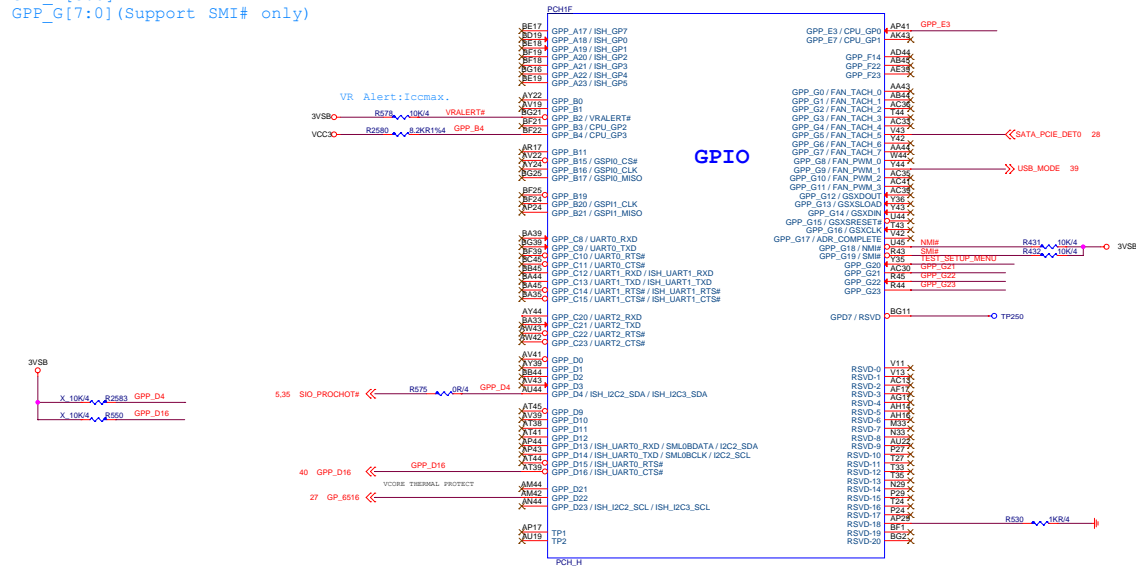




RTC Block

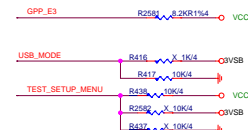


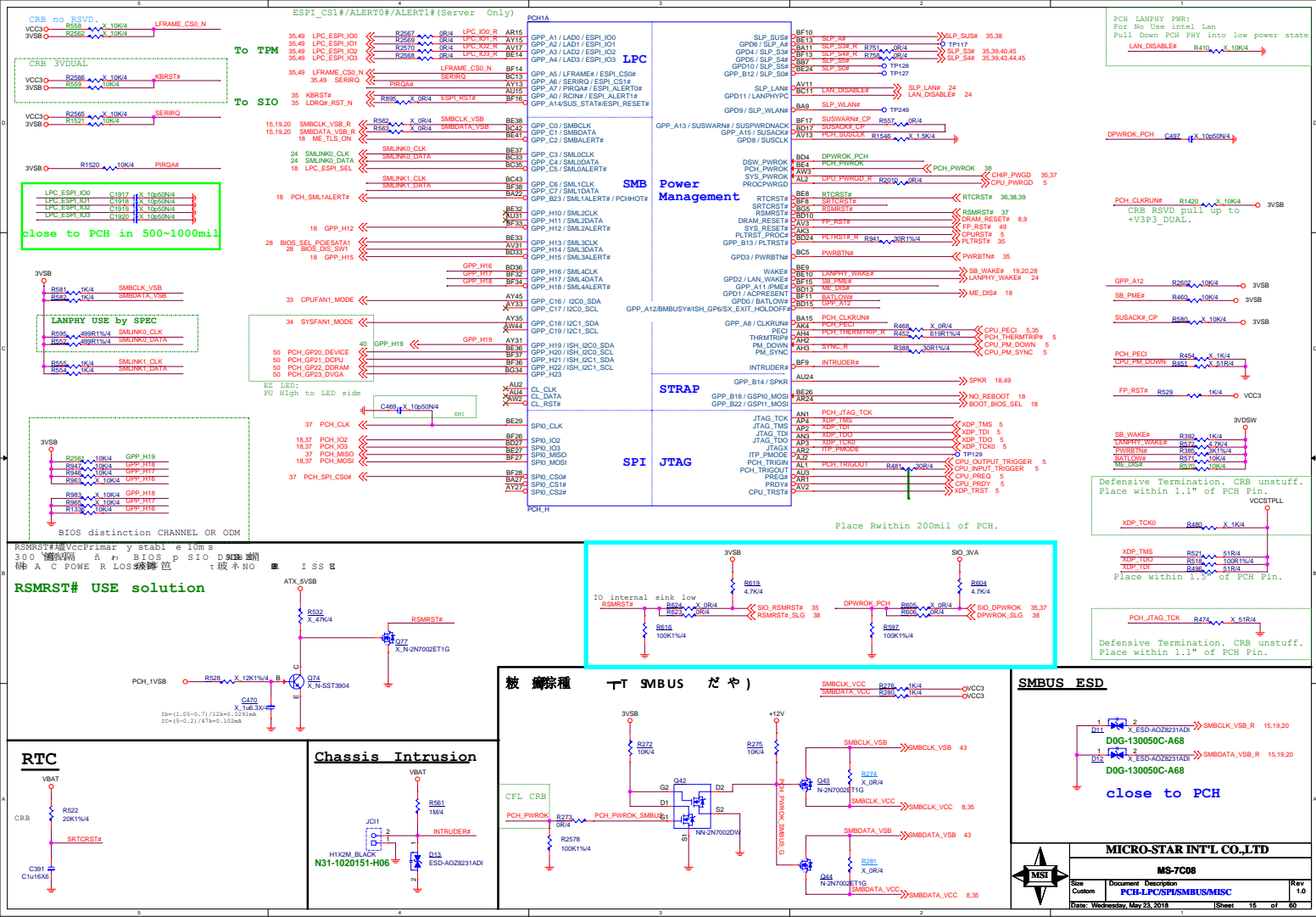
```
GPIO(SMI/NMI):
GPP_B14,GPP_B20,GPP_B23
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]
GPP_I[3:0]
GPP_G[7:0] (Support SMI# only)
```

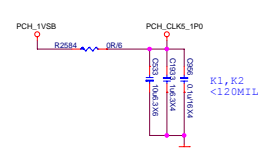


	GPP_I12	GPP_I13	GPP_I14
H310_GPLUS	0	0	0

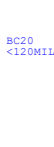
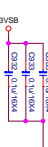
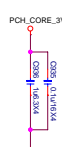
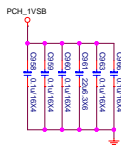
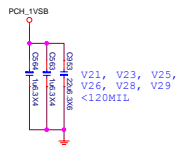
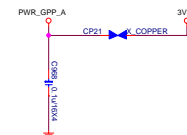
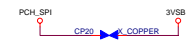
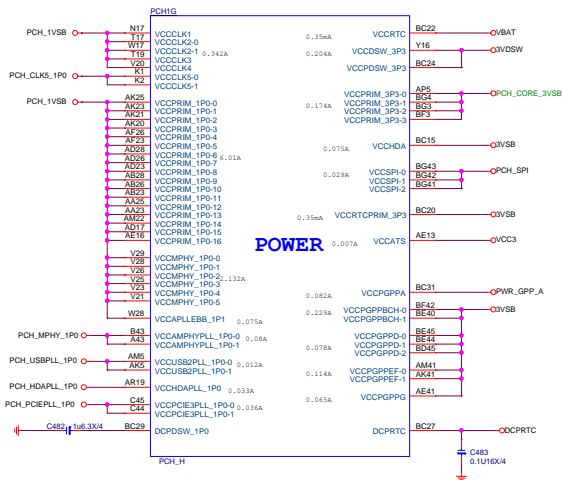
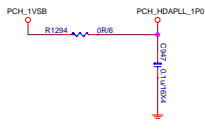
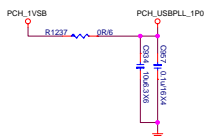
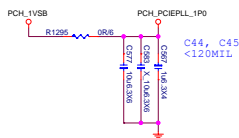
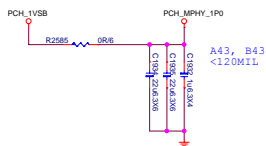
For BIOS BOM USE







```
PCH_1VSB 8.72A
VCC3 0.007A
3VSB 0.846A
```



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Size Custom	Document Description PCH-Power	Rev 1.0
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PCMH	K27	
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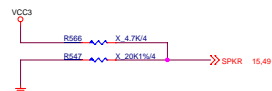
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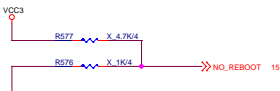
Size Custom	Document Description PCH-GND	Rev 1.0
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TOP Swap



Internal pull-down 20K is disabled after PLTRST#

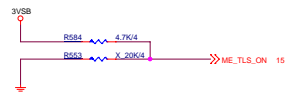
No Reboot



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1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

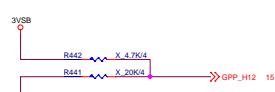
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

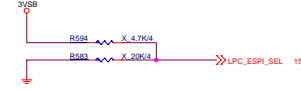
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

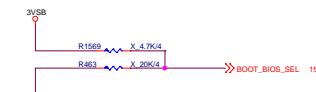
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

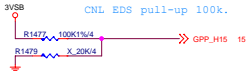
Boot BIOS



0 : SPI
1 : LPC

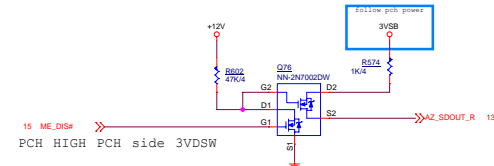
Internal pull-down 20K is disabled after PLTRST

Reserved



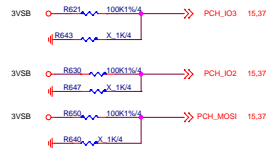
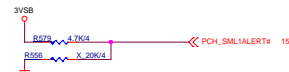
HDA_SDO

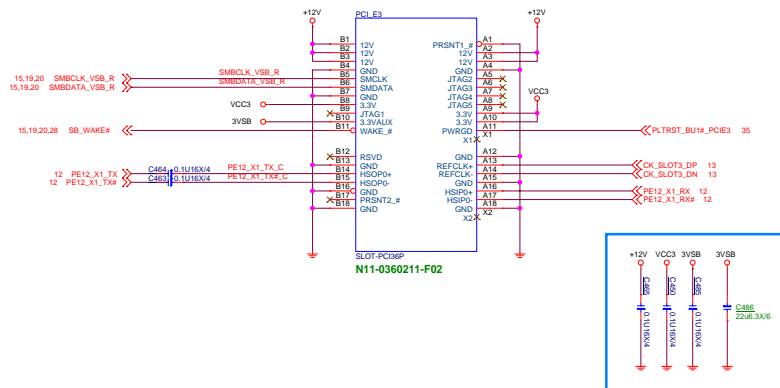
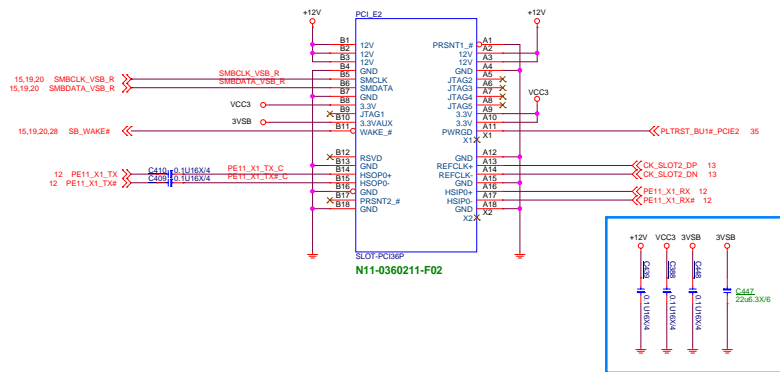
ME flash by GPIO



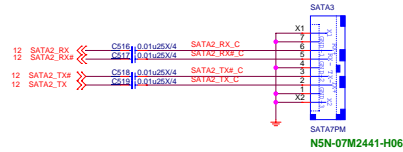
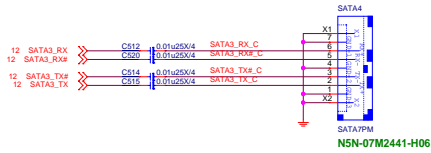
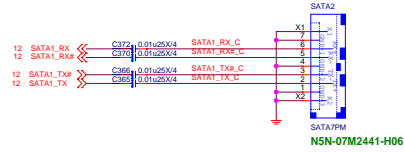
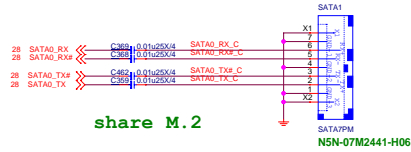
15 ME_DISF >>> PCH HIGH PCH side 3VDSW

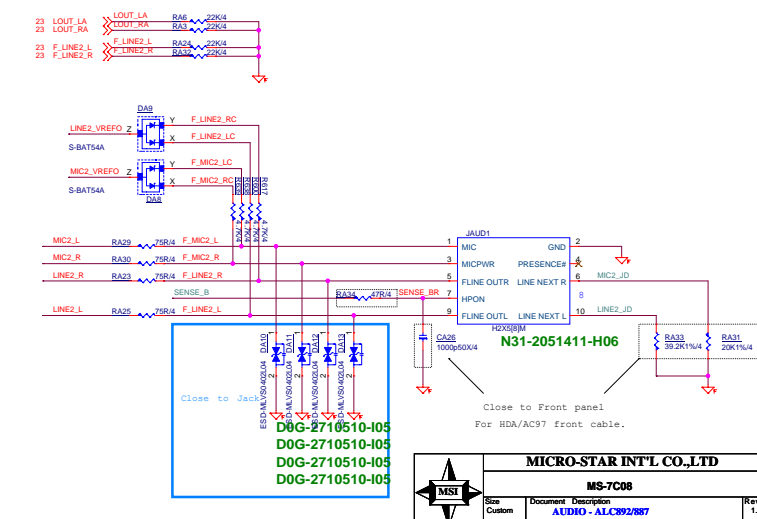
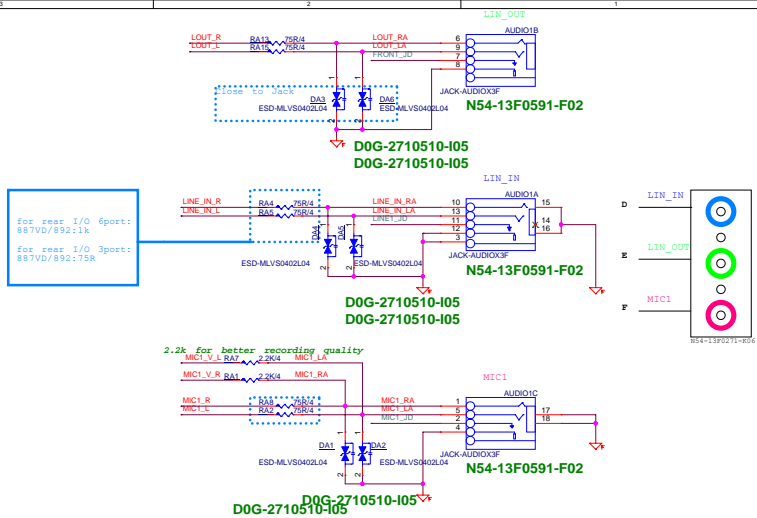
Reserved





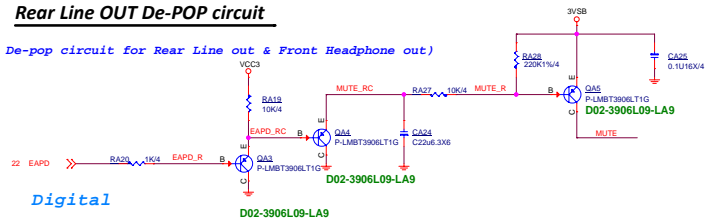
SATA 6G





Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

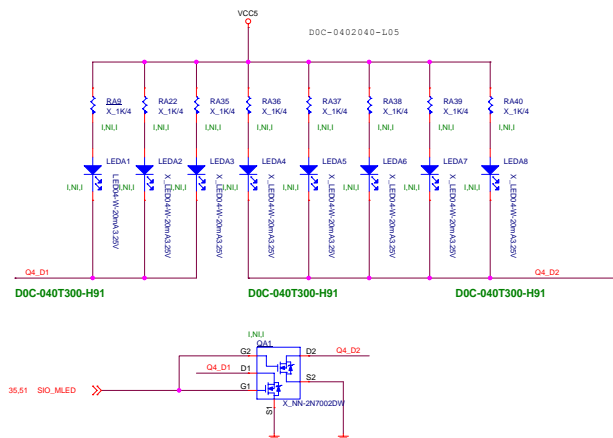


Analog

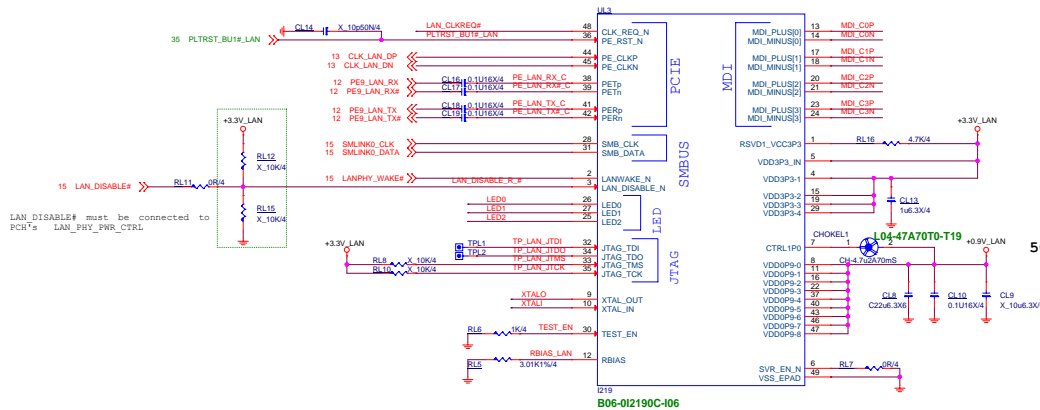


Audio most is transparent and width 40mil

Audio LED



Intel Lan- I219

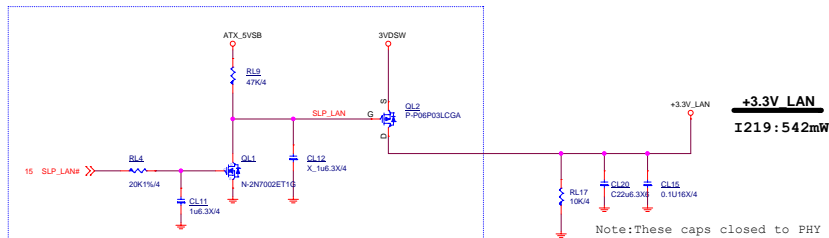


PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

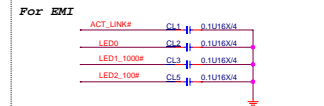
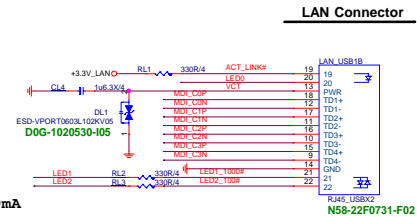


The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKREQ<n> buffer.

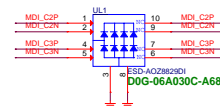
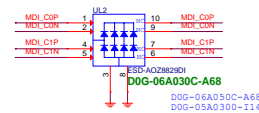
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



Note: These caps closed to PHY



UL2&UL3 close to connector



Do not pair MDIO and MDI1 on the same TVSdevice
(avoid LAN POE connecting issue).
Otherpairing combination is ok.

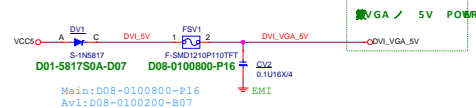
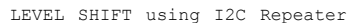
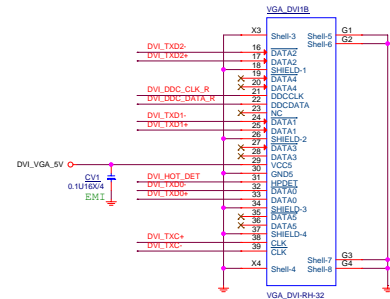
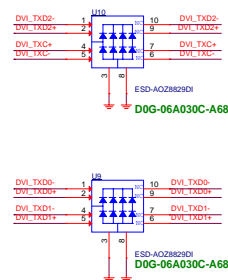


MICRO-STAR INT'L CO.,LTD

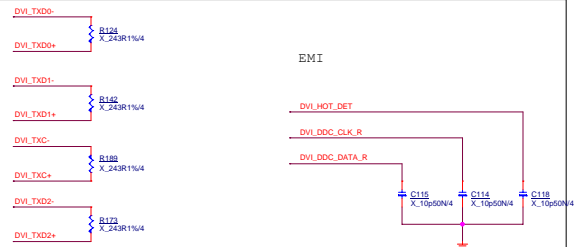
MS-7C08

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VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



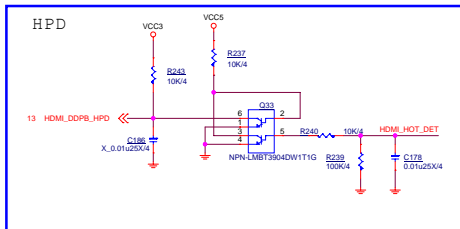
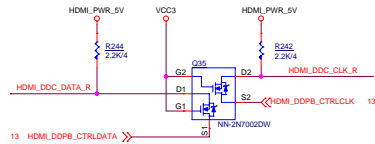
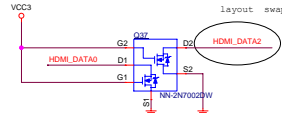
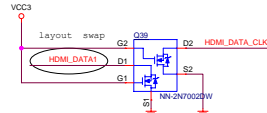
EMI



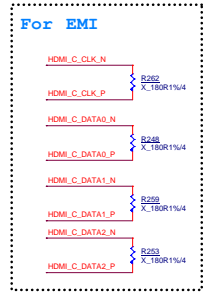
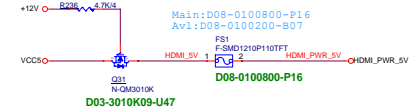
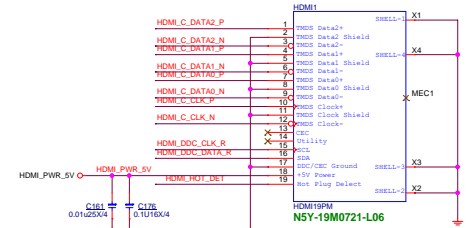
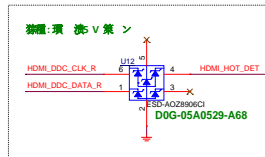
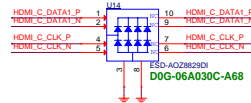
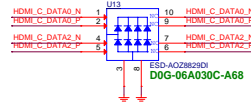
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HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



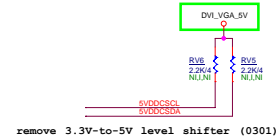
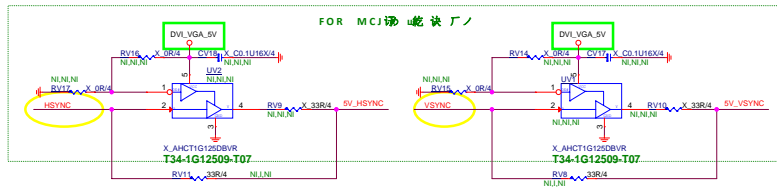
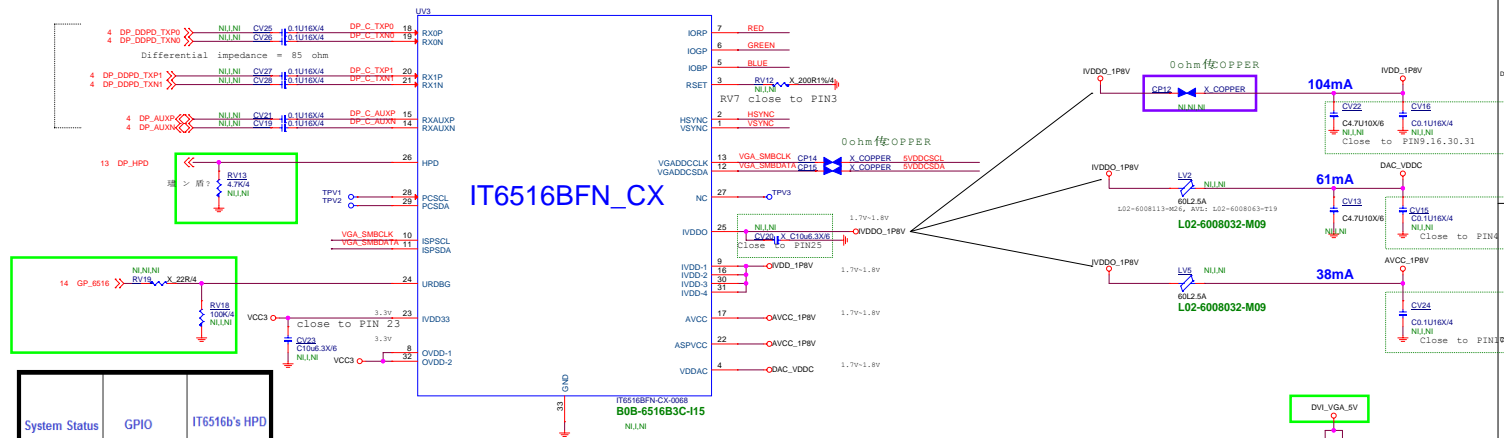
- 1



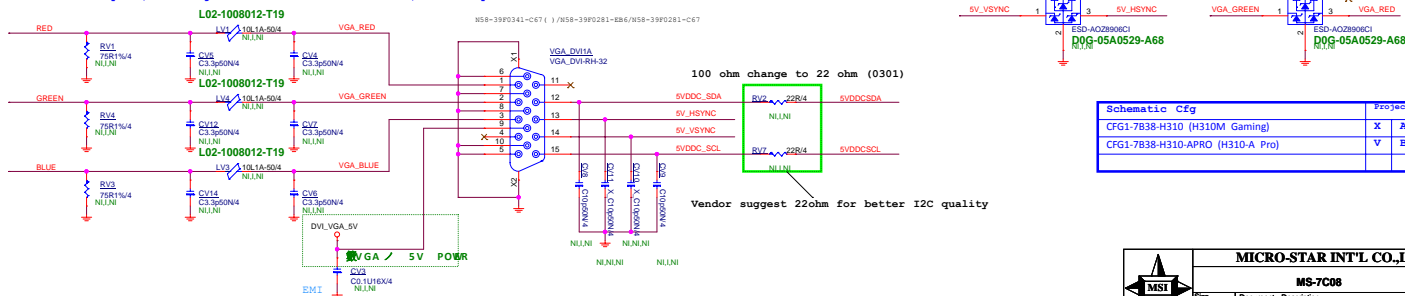
MICRO-STAR INT'L CO.,LTD			
MS-7C08			
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Note:
If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining

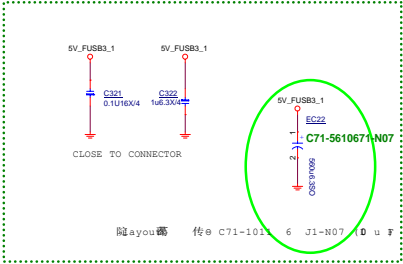
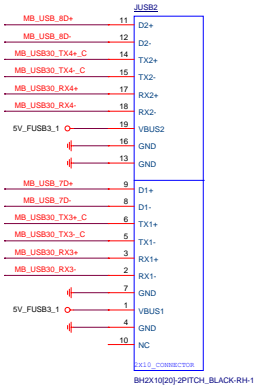
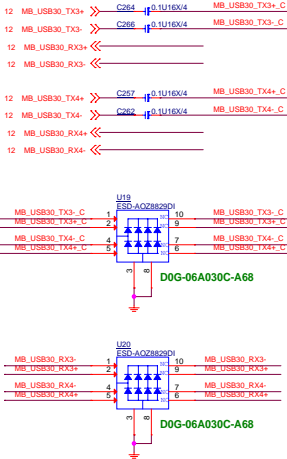
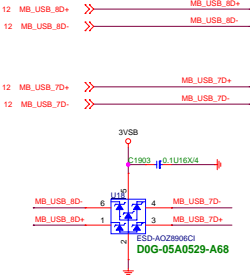


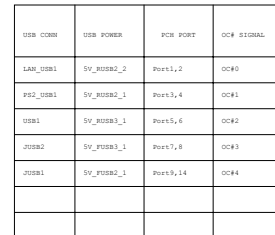
If have VSIS1.2 SPEC request, can change head to L02-2208012-M09 use, It test pass.



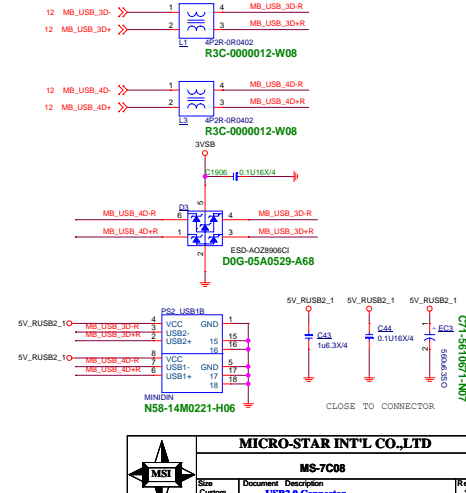
Schematic Cfg		Project
CFG1-7B38-H310 (H310M Gaming)	X	A
CFG1-7B38-H310-APRO (H310-A Pro)	V	B

Front JUSB3 port 7,8

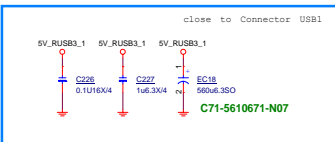
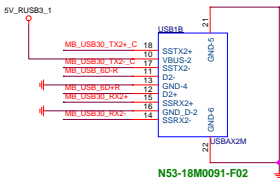
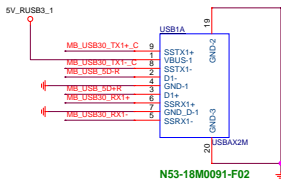
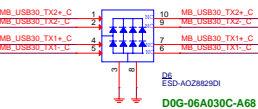
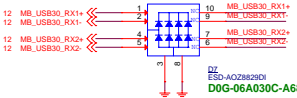
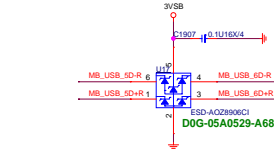
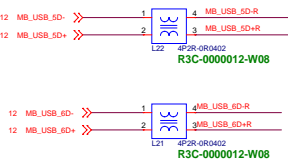




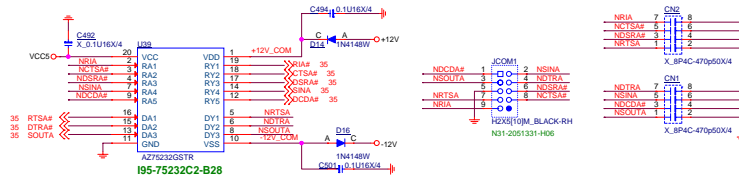
PS2_USB1 PORT 3,4



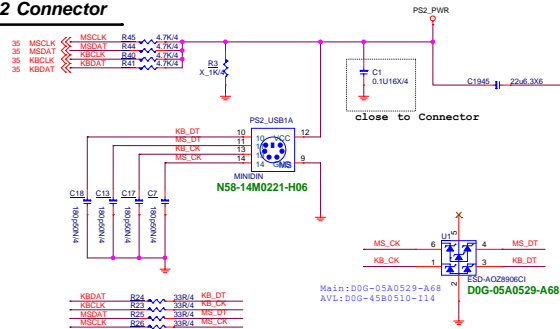
REAR USB1 Connect



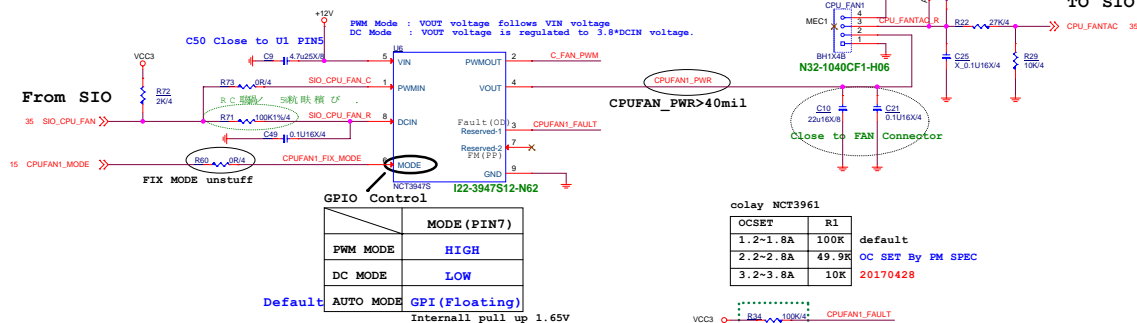
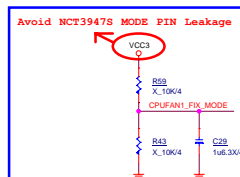
SERIAL PORT 1



PS2 Connector



GPIO パス ち伝 PW M/DC MO DE



OCSET	R1
1.2~1.8A	100K
2.2~2.8A	49.9K
3.2~3.8A	10K

Avoid NCT3947S MODE PIN Leakage

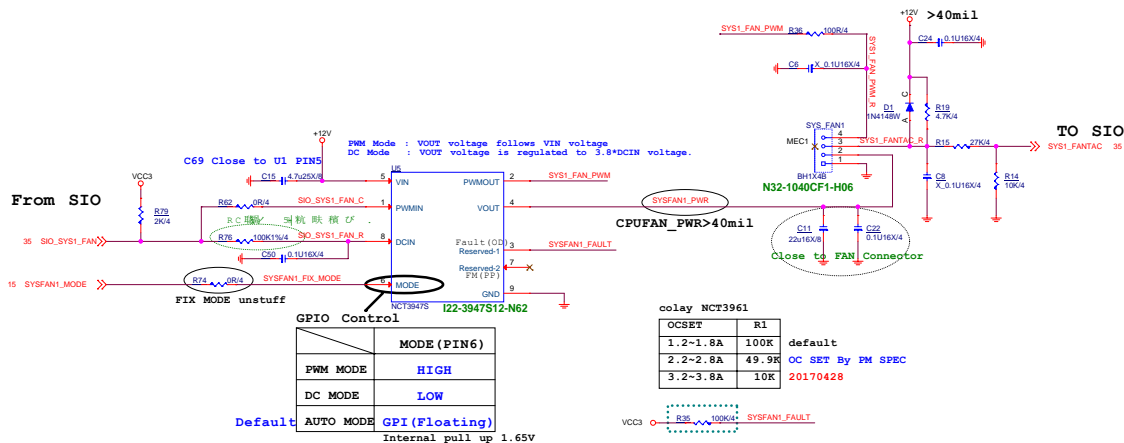
VCC3

R81
X_10K/4

SYSFAN1_FIX_MODE

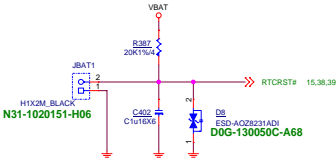
R82
X_10K/4

C56
1u6.3X/4

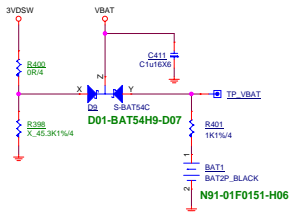


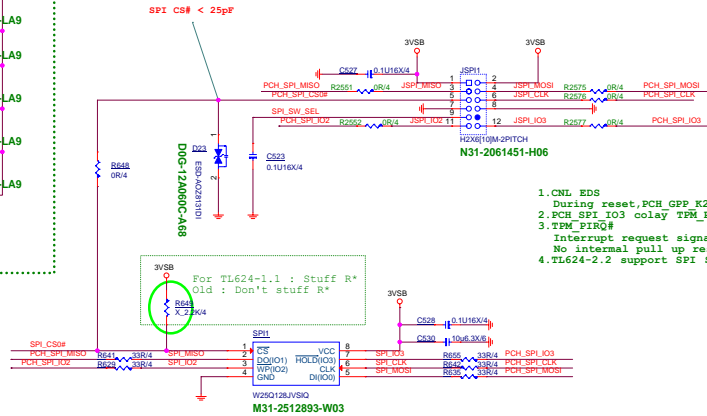
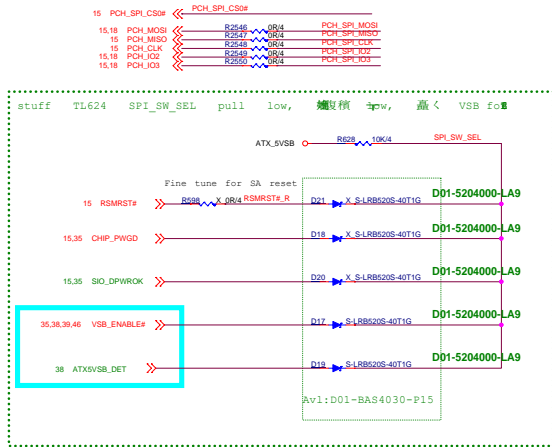
OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By FM SPEC
3.2~3.8A	10K	20170428

Cut VBAT

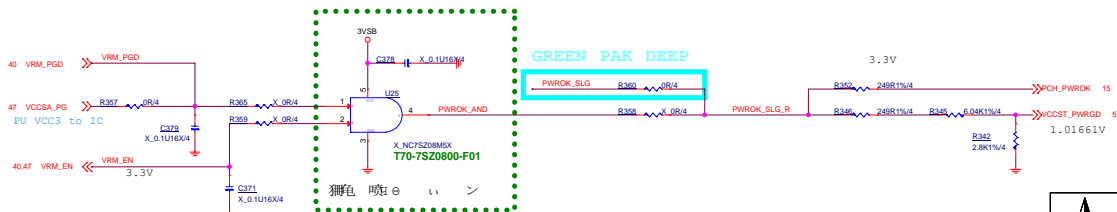
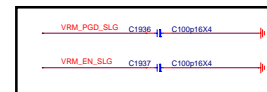
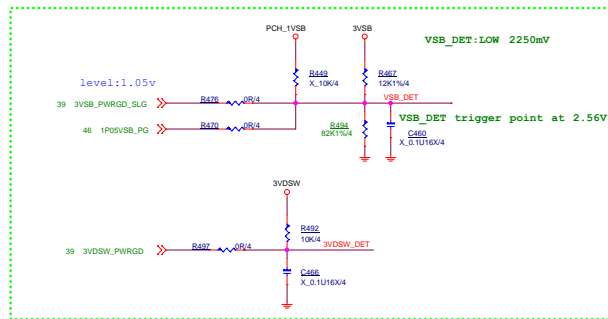
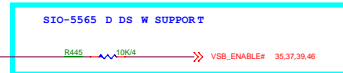
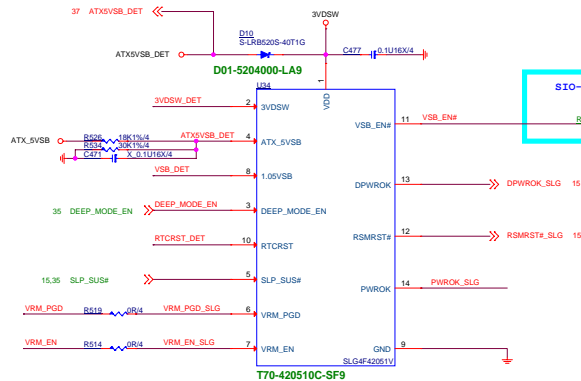
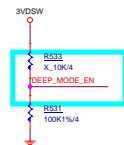
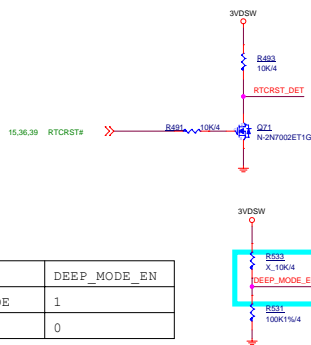


VBAT

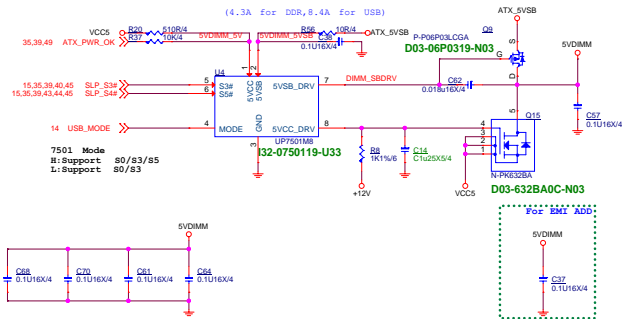




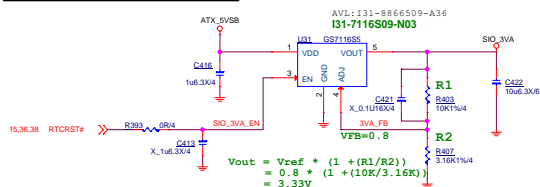
	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0



5VDIMM@5V/11. 3075A

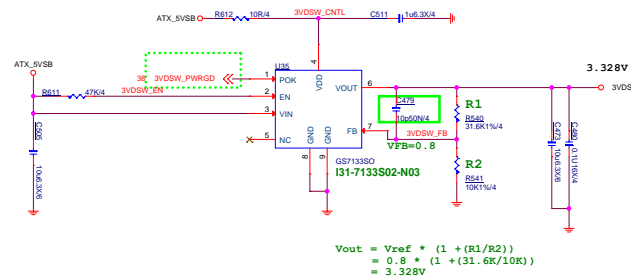


SIO 3VA@3.3V/20mA

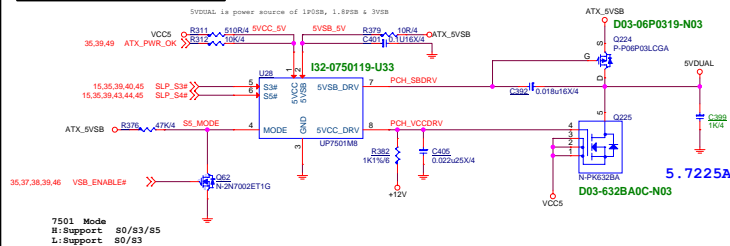


3VDSW@3.3V/0.3A

Intel Lan 113mA (PCH) + 0.6mA (RTC) + 200mA (LAN-I219) + SIO

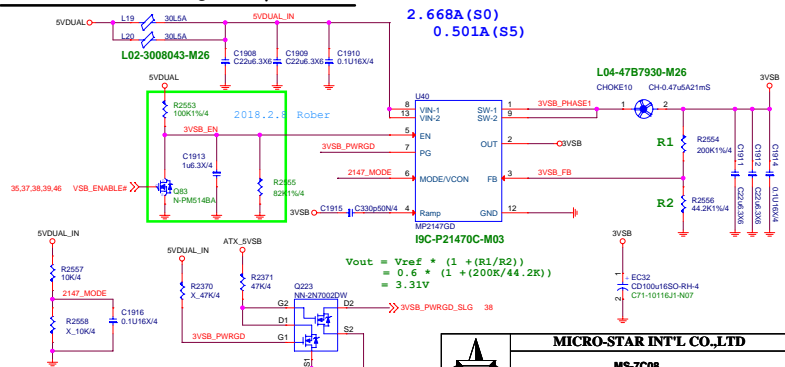


5VDUAL@5V/5. 7225A



3VSB cost down@3.3V/3.281A

2.253A (PCH) + 0.415A (PE SLOT*3)
2.668A (S0)
0.501A (S5)

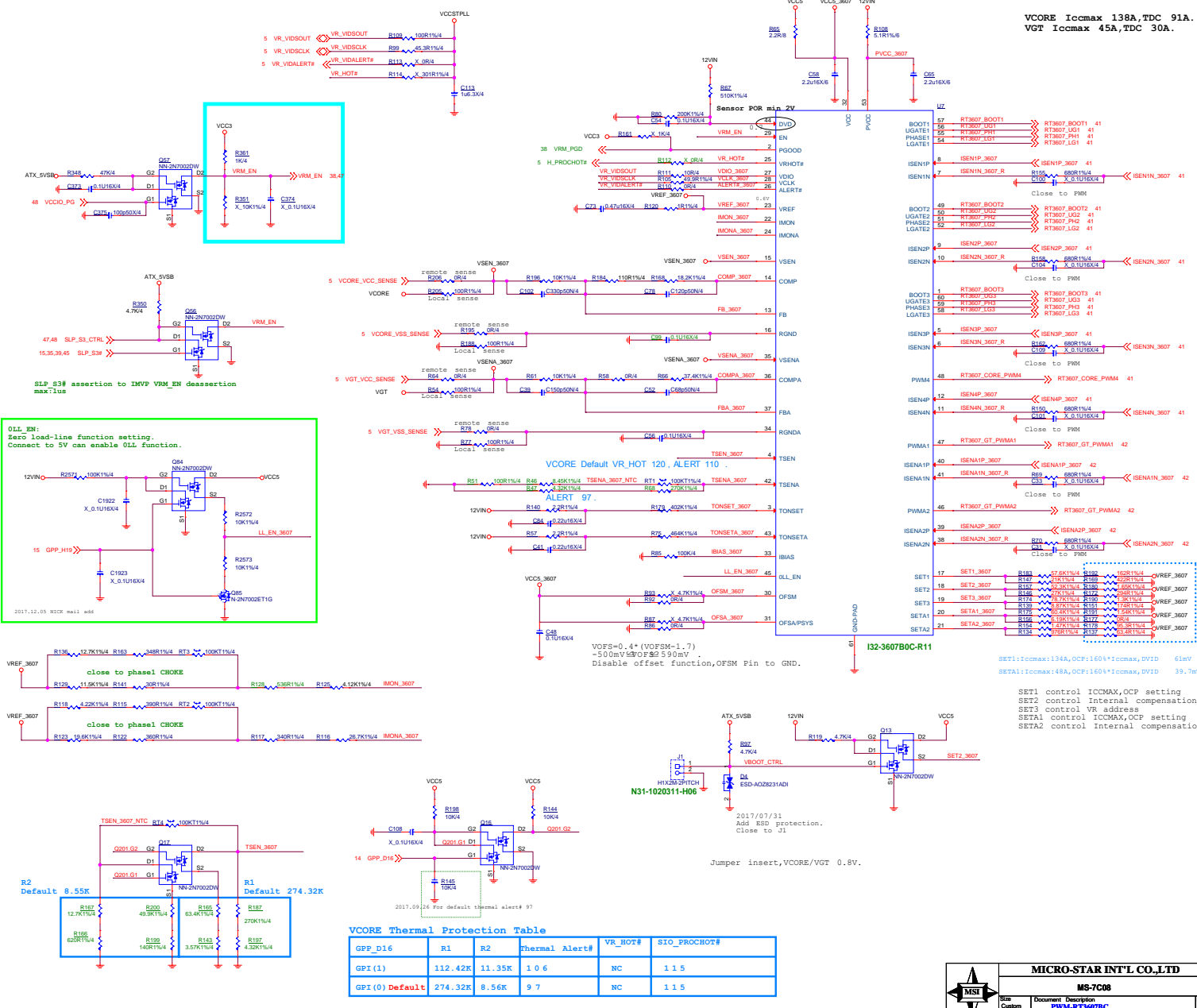


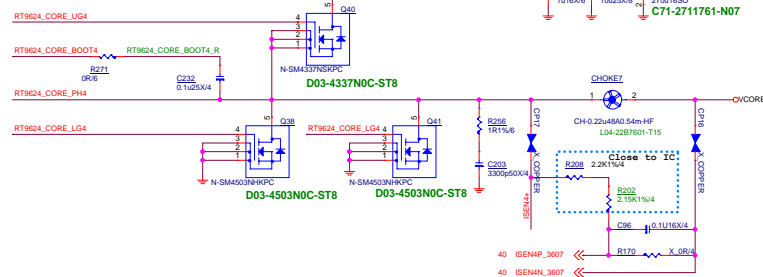
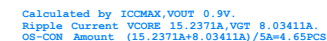
MICRO-STAR INT'L CO.,LTD

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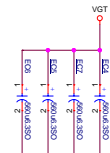
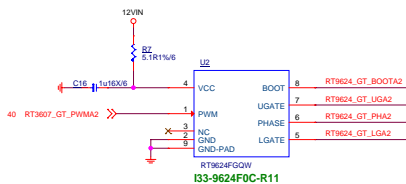
Rev	Description	Date
1.0	ACPI CONTROLLER	Wednesday, May 23, 2018

VCORE Iccmax 138A,TDC 91A.
VGT Iccmax 45A,TDC 30A.





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VCC_DDR@1.2V/11.525A

DDR4_1.2V 3.3A+ 7.85A+0.375A=11.525A

3.3A FOR CPU
10A FOR ZDIMM DDR4
0.375A FOR VTT_DDR

b03-632BA0C-N03 3~4.6mohm/4.5V
Current limit= 174K*5uA/3.9mohm)= 22.3A
Current limit= 174K*5uA/5.1mohm)=17.1A
OUTPUT CHOCKE Isd=32A
Vcs=174K*5uA=0.87V(Spec:0.4V~3V)

4503 Rdsn

10V 2.5~3mohm

4.5V 3.9~5.1mohm

Vout=0.75V/1.65K*(1.65K+1K)=1.204V

NCT3933 source 10uA

Vout=[VREF*(1+R171/R153)]+10uA*R171
=0.75V*(1+1K/1.65K)+10uA*1K=1.204V+0.010V=1.215V

NCT3933 sink 10uA

Vout=[VREF*(1+R171/R153)]-10uA*R171
=0.75V*(1+1K/1.69K)-10uA*1K=1.204V-0.010V=1.195V

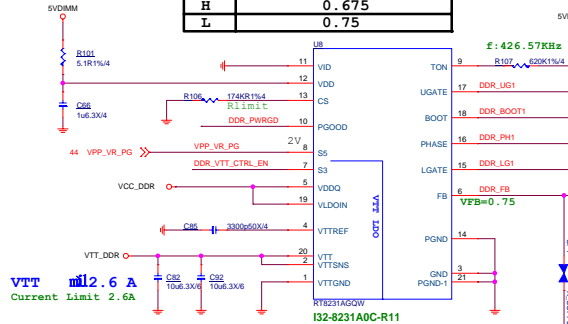
Iin=IOCP*Vout/08/Vin

=22.3A*1.2V/0.8/5V=6.69A

L02-3008043-M26

Over 85 , Rated Current 1.5A

VID	Reference Voltage (V)
H	0.675
L	0.75



$$V_{out} = V_{ref} * (1 + (R1/R2))$$

$$= 0.75 * (1 + (1K/1.65K))$$

$$= 1.204V$$

$$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in})) * (1 - (V_{out}/V_{in}))}$$

$$= 11.525 * 0.427$$

$$= 4.921A$$

$$L = t_{ON} * (V_{IN} - V_{DDQ}) / (LIR * I_{LOAD}(MAX))$$

$$t_{ON} = 636.4456ns$$

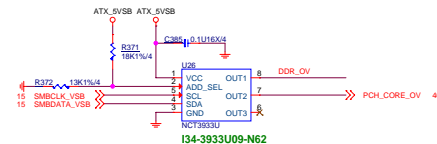
$$LIR = 20\% \sim 40\%$$

$$L = 0.63uH \sim 1.27uH$$

MAX: 11.525A
1.2V

UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K



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VPP25 @2.5V/2A

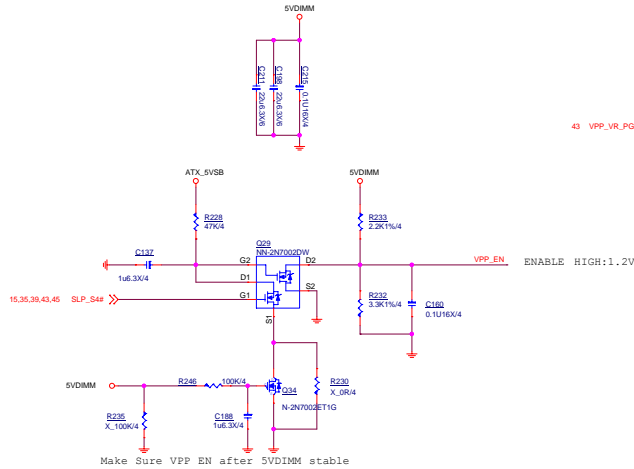
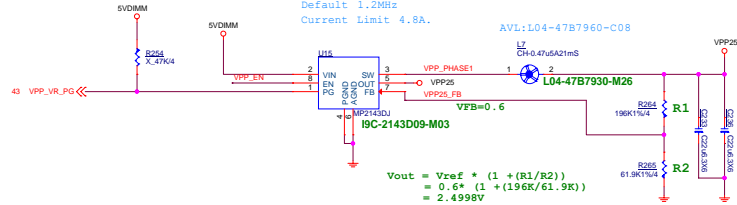
2DIMM :1.12A FOR
DDR VPP2.5V

DDR VPP m14.8

Switch Frequency
Default 1.2MHz
Current Limit 4.8A.

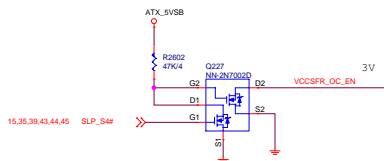
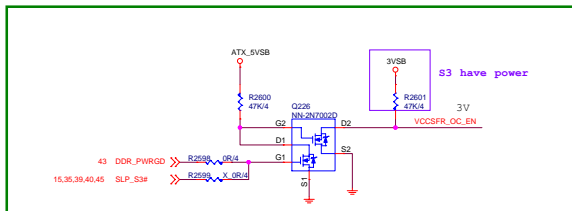
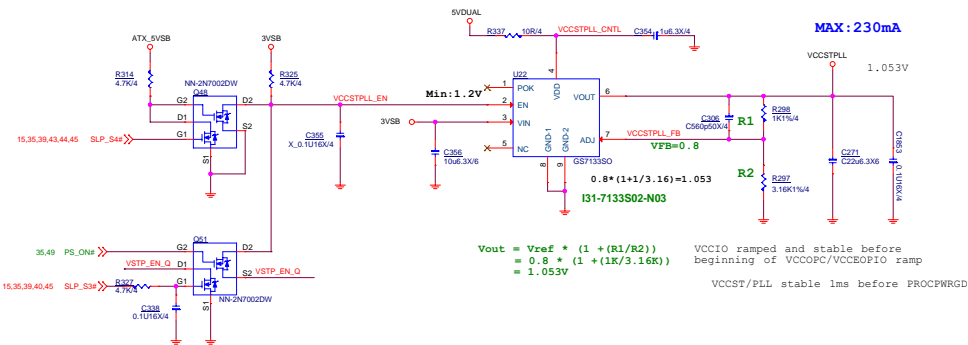
Input Current= (2A*2.5V)/5V/0.8=1.25A

AVL:L04-47B7960-C08



Make Sure VPP EN after 5VDIMM stable

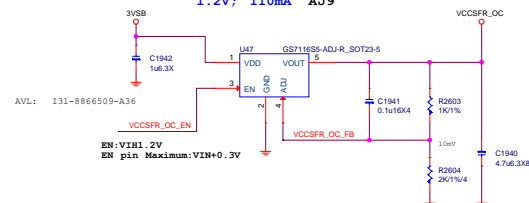
VCCSTPLL@1.05V/230mA



from NCT3933

VCCPLL OC

1.2V; 110mA AJ9



PCH 1VSB@1V/8.72A

4503 Rds(on)
10V 2.5~3mohm
4.5V 3.9~5.1mohm

Current limit= $6.65K \cdot 10uA / 3.9mohm = 17.05A$
Current limit= $6.65K \cdot 10uA / 5.1mohm = 13.04A$
CHOKE Isat=18A
From CHOKE I-L Curve, when $I=25A$, $L=0.6uH$.

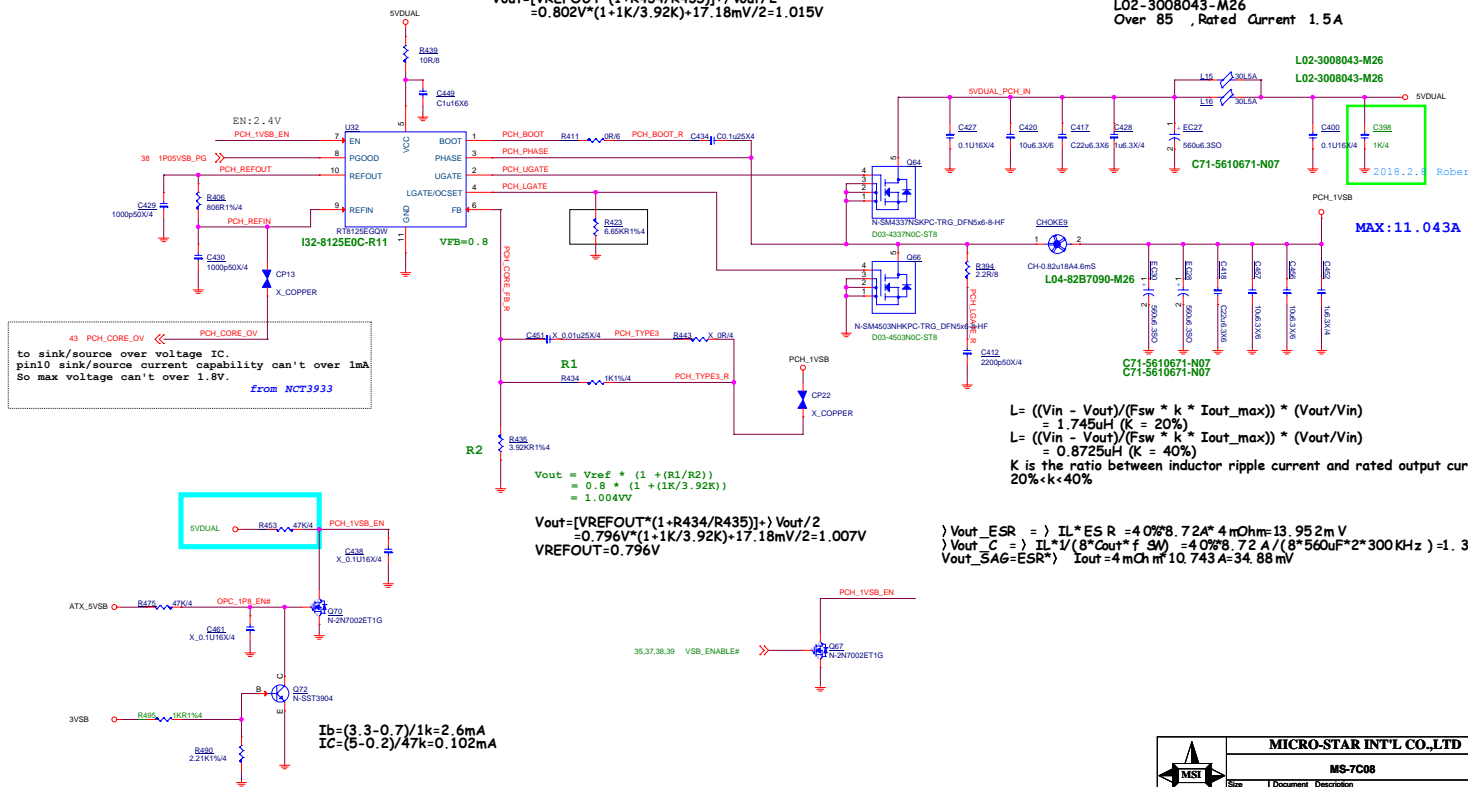
Default Vout=1V

NCT3933 sink 10uA
 $VREFIN = VREFOUT - 10uA \cdot R406 = 796mV - 8mV = 788mV$
 $Vout = [VREFOUT \cdot (1 + R434/R435)] \cdot Vout / 2$
 $= 0.788V \cdot (1 + 1K / 3.92K) \cdot 17.18mV / 2 = 0.997V$

NCT3933 source 10uA
 $VREFIN = VREFOUT + 10uA \cdot R407 = 796mV + 8mV = 804mV$
 $Vout = [VREFOUT \cdot (1 + R434/R435)] \cdot Vout / 2$
 $= 0.802V \cdot (1 + 1K / 3.92K) \cdot 17.18mV / 2 = 1.015V$

$I_{rms} = I_{out} \cdot \sqrt{(V_{out}/V_{in}) \cdot (1 - (V_{out}/V_{in}))}$
 $= 8.72 \cdot 0.276$
 $= 2.407A$

$I_{in} = I_{OCP} \cdot V_{out} / 0.8 \cdot V_{in}$
 $= 17.05A \cdot 1V / 0.8 \cdot 5V = 4.2625A$
L02-3008043-M26
Over 85 , Rated Current 1.5A



4503 Rdson
10V 2.5~3mohm
4.5V 3.9~5.1mohm

Current limit= $5.1\text{K} \times 10\mu\text{A} / 2.5\text{mohm} = 20.4\text{A}$
 Current limit= $5.1\text{K} \times 10\mu\text{A} / 3\text{mohm} = 17\text{A}$
 CHOKE Isat=17A
 From CHOKE I-L Curve, when I=25A, L=0.6uH

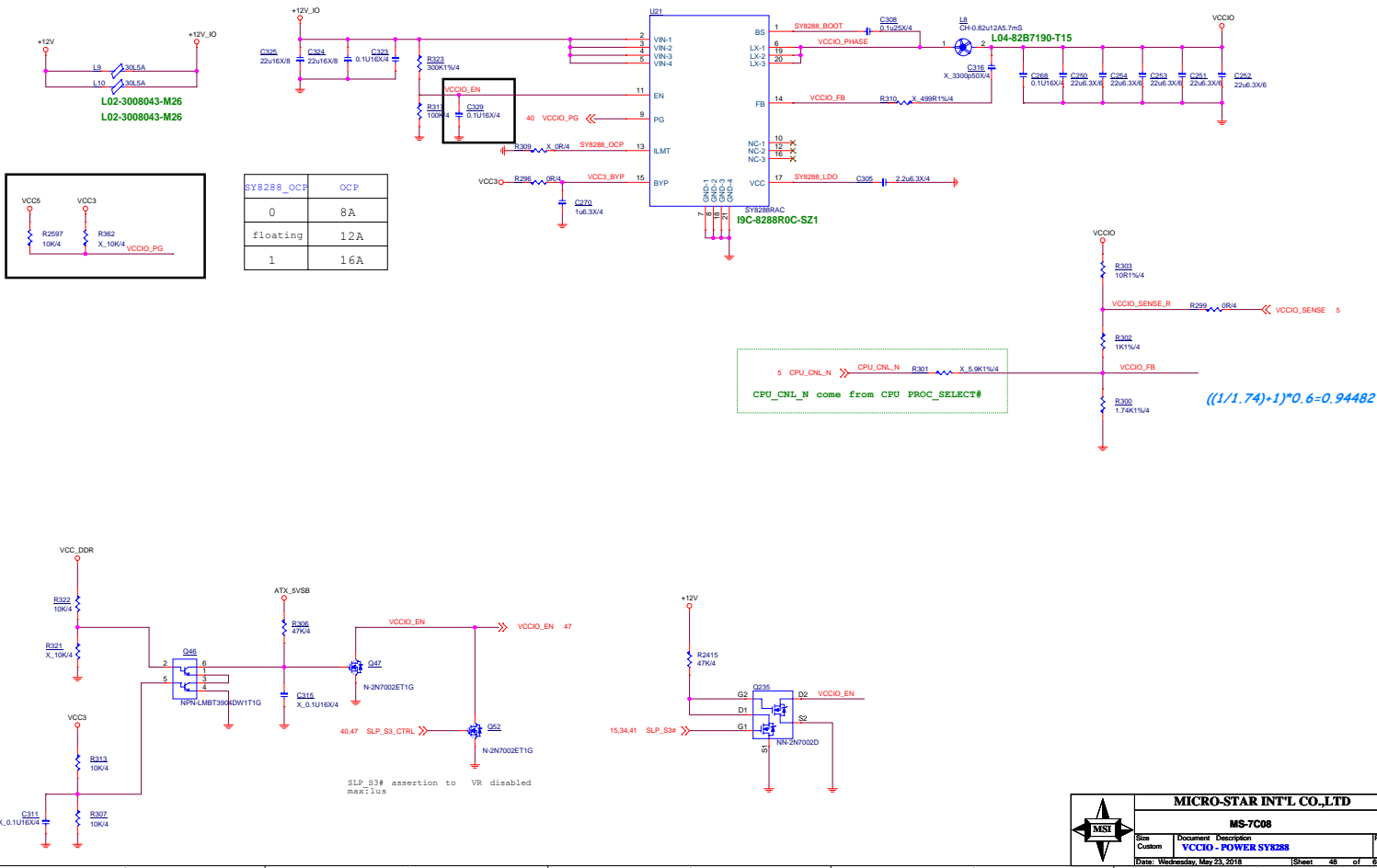


VCCIO@0.95V/6.4A

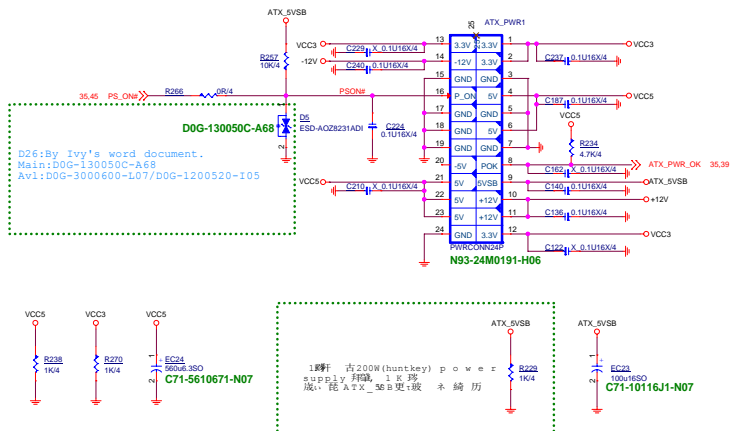
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT*40%*IMAX/2=12A~14A.

VCCIO m112A(floating)

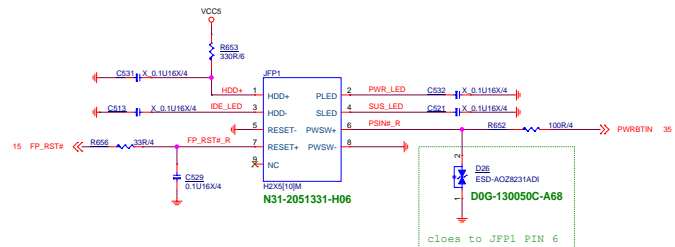
MAX: 6.4A



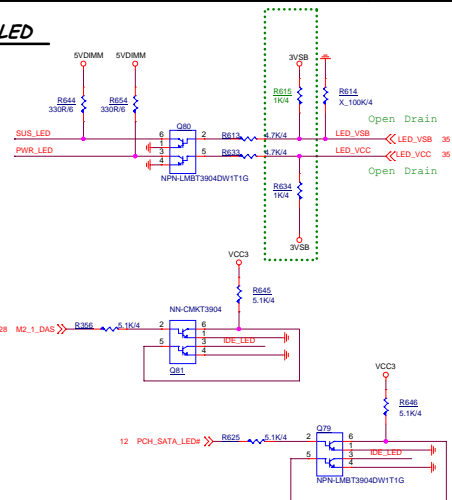
ATX POWER CONNECTOR



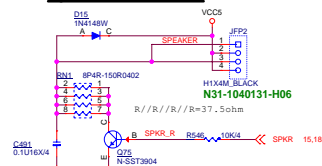
FRONT PANNEL



LED



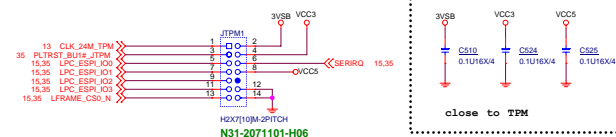
Speaker Pin Header



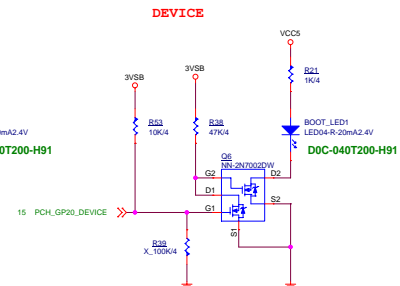
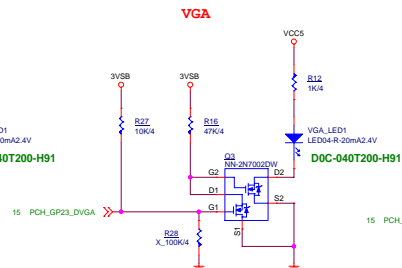
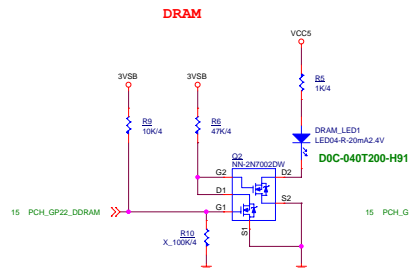
$$I_b = (5 - 0.7) / 37.5 = 0.1146 \text{ mA}$$

$$I_c = (5 - 0.2) / 10 \text{ k} = 0.48 \text{ mA}$$

TPM



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LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
獵	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
防	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

LED
RED:D0C-040P100-H91
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91
AVL:D0C-040S200-E07

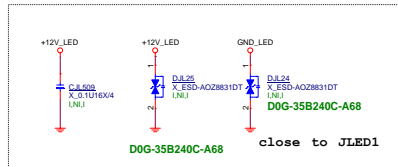
网劫案第3渔LED蛾default稽诈诀窃读
1. 健CPU check CPU LED 猎checkRASS 读弱LED防奔
2. 便利m emory /m emoji 猎checkPASS m em or y
LED 防奔
3. VGA check/VGA LED 猎che ck PS读明 VG 弊
4. 程决饵料 诈诀 LED 猎端邪罪
参非市尤符研 参非决班LED端邪罪



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unstuff



CPU_H1
E21-7557050-L06



BAT1_X1
BAT18CR032P

D06-0100101-K26



HDMI LABEL

Y01-RHDMI03-000



BIOS_LA1
AMI

G51-M1SPXXA-A09



LA10
NKT

Y02-MU00170-CFO

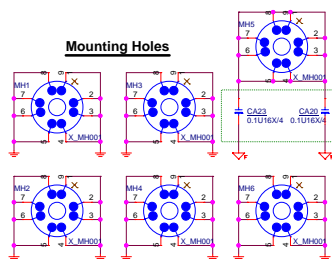
Optical Fiducial Marks-120



Simulation



Mounting Holes



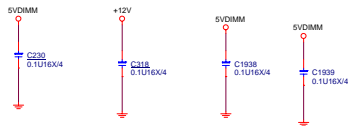
HOLES_4S

VPP25	TP_VPP25
VTT_DDR	TP_VTT_DDR
5VDIMM	TP_5VDIMM
3VSB	TP_3VSB
3VDSW	TP_3VDSW
VGT	TP_VGT
VCCSTPLL	TP_VCCSTPLL
VCCIO	TP_VCCIO
VCCSA	TP_VCCSA
VCC_DDR	TP_VCC_DDR
PCH_1VSB	TP_PCH_1VSB_VSB
SIO_3V/A	TP_SIO_3V/A

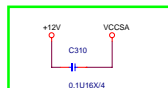
Near SIO CHIP

+12V	TP_+12V
VCORE	TP_VCORE
VCC5	TP_VCC5

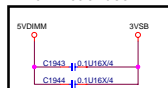
return path



For M2 reference +12V USE
please close to under M2



for most use



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